WHAT IS CLAIMED IS:

1. A chip package, comprising:

a chip, having an active surface and a plurality of bond pads, said bond pads being on said active surface; and

a rigid cover, on said active surface, said rigid cover exposing said plurality of bond pads above said active surface.

2. The chip package of claim 1, wherein said chip includes a redistribution layer on said active surface to form said plurality of bond pads.

3. The chip package of claim 1, wherein said rigid cover is adhered to said active surface.

4. The chip package of claim 1, wherein said rigid cover having a periphery adhered to said active surface.

5. The chip package of claim 1, wherein the material of said rigid cover includes a conducting material, an insulating material, or a transparent material.

6. The chip package of claim 1, further comprising a plurality of contacts on said plurality of bond pads respectively, the heights of said contacts relative to said active surface are larger than the height of said rigid cover relative to said active surface.

7. The chip package of claim 1, wherein said plurality of bond pads is disposed on the circumference of said active surface.

8. The chip package of claim 7, wherein said active surface is a rectangle, and said plurality of bond pads are disposed on one side outside of said rectangle.

9. The chip package of claim 7, wherein said chip has a backside relative to said active surface and a plurality of connecting lines, each of said plurality of connecting lines having an end connected to one of said plurality of bond pads, said plurality of

connecting lines extending to said backside via a lateral side of said chip and forming a plurality of terminal pads on said backside respectively.

10. The chip package of claim 9, wherein said plurality of terminal pads is disposed on the circumference of said backside.

11. The chip package of claim 9, wherein said plurality of terminal pads is disposed on said backside of said chip as an area array.

12. The chip package of claim 9, wherein said lateral side of said chip includes a concave surface and portions of said connecting lines are on said concave surface respectively.

13. The chip package of claim 9, further comprising a plurality of contacts on said terminal pads respectively.

14. The chip package of claim 1, wherein said plurality of bond pads are disposed on said active surface as an area array, said rigid cover having a plurality of openings to expose said bond pads respectively.

15. A chip packaging process, comprising:

providing a wafer, said wafer having an active surface and a backside corresponding to said active surface, said wafer having a first chip area and a second chip area adjacent to said first chip area, said wafer having a plurality of first and second bond pads on said active surface in said first and second chip areas respectively;

forming a plurality of through holes on said wafer, said plurality of through holes passing through said wafer and connecting said active surface and said backside, said through holes being arranged between said first chip area and said second chip area;

forming a plurality of first and second connecting lines on said wafer, each of said plurality of first connecting lines having a first end through one of said plurality of

through holes electrically connected to one of said plurality of first bond pads, each of said plurality of first connecting lines having a second end extending to said backside of said first chip area to form one first terminal pad on said backside of said first chip area, each of said plurality of second connecting lines having a first end through one of said plurality of through holes electrically connected to one of said plurality of second bond pads, each of said plurality of second connecting lines having a second end extending to said backside of said second chip area to form one second terminal pad on said backside of said second chip area, portions of said first connecting lines in said through holes being connected to portions of said second connecting lines in said through holes respectively;

disposing a first rigid cover and a second rigid cover on said active surface of said first chip area and said active surface of said second chip area respectively;

sawing said wafer along an area between said first and second chip areas and sawing said portions of said first connecting lines in said through holes and said portions of said plurality of second connecting lines in said through holes; and

separating said first chip area and said second chip area from said wafer, said first chip area and said first rigid cover being a first chip package, said second chip area and said second rigid cover being a second chip package.

16. The process of claim 15, before said step of separating said first chip area and said second chip area from said wafer, further comprising forming a plurality of contacts on said first and second terminal pads.

17. The process of claim 15, wherein said first rigid cover is adhered to said active surface.

18. The process of claim 15, wherein the periphery of said first rigid cover is

adhered to said active surface.

19. The process of claim 15, wherein the material of said first rigid cover includes a conducting material, an insulating material, or a transparent material.

20. The process of claim 15, wherein said plurality of first terminal pads are disposed on the circumference of said backside of said first chip area.

21. The process of claim 15, said plurality of first terminal pads are disposed on said backside of said first chip area as an area array.

22. The process of claim 15, wherein forming said portions of said plurality of first connecting lines in said plurality of through holes are performed by electroplating.

23. The process of claim 15, wherein said first and second rigid covers are structural connected, said step of sawing said wafer further comprising sawing said structural connection of said first and second rigid covers to separate said first and second rigid covers.